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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,007	02/02/2001	Hsingya Arthur Wang	00939A045100	5469

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EXAMINER

ROSE, KIESHA L

ART UNIT PAPER NUMBER

2822

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/777,007

Applicant(s)

WANG ET AL.

Examiner

Kiesha L. Rose

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**: 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 6-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

### DETAILED ACTION

This Office Action is in response to the RCE filed 26 April 2004.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. Patent 5,468,981) in view of Gill (U.S. Patent 5,418,741) and Stewart (U.S. Patent 4,185,319).

Hsu discloses an EEPROM (Fig. 1) that contains a p-type semiconductor substrate (12), an n-type drain region (14) formed into substrate, an n-type double diffused source region (16) comprising a first sub-region (18) of a first dopant species (arsenic) with a first distance and a second sub-region (20) of a second dopant species (phosphorous) with a second distance formed in substrate in spaced alignment with drain region with a channel region (30) therebetween, where source region has a more abrupt profile grade relative to the surface than drain region, where source and drain form a pn junction with the substrate, a floating gate electrode (24) located over channel region and having a portion over both the drain and source regions wherein a greater portion is over the source region and a control gate electrode (26) overlapping floating

gate electrode. Hsu discloses all of the limitations except for word lines and bit lines. Whereas Gill discloses an EEPROM (Fig. 1A) that contains a plurality of memory cells arranged in a matrix of N-rows (word lines) and M-columns (bit lines), a plurality of floating gate transistors all containing a control gate (14), a floating gate (13), a source (12) and a drain (11), word lines (15) connect together the control gates in a common row, bit lines (17) connect the drains of the transistor in common column and a common node (19) connecting the source regions together, the first transistor stores one bit of data and the second transistor configured to store another bit of data. The word and bit lines are formed to connect the control gates of plurality of transistors together and the plurality of drain regions together. Since Hsu and Gill are both from the same field of endeavor, EEPROM, the purpose disclosed by Gill would have been recognized in the pertinent art of Hsu. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the EEPROM of Hsu by incorporating a bit and word line to connect the plurality of control gates and drain regions together as taught by Gill. Hsu and Gill disclose all of the limitations except for the control gate to have one voltage and the source to have another and the drain grounded. Whereas Stewart discloses a memory device (Fig. 4) that discloses that in the programming mode of the memory device the control gate has one voltage, the source has another voltage (positive) and the drain is grounded. The control gate and source region have a positive voltage and the drain region is grounded to put the memory device in program mode. (Column 4, lines 36-46) Since Hsu, Gill and Stewart are both from the same field of endeavor, memory devices, the purpose disclosed by Stewart would have been

recognized in the pertinent art of Hsu and Gill. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Hsu and Gill by incorporating the control gate and source region to have a positive voltage and the drain region to be grounded to put the memory device in program mode as taught by Stewart. In regards to claims 18 and 24-25, Hsu, Gill and Stewart disclose the claimed invention except for the first voltage to be about 8.5 volts and the second voltage to be about 4.5 volts and the first distance of the source region is 0.1 microns and the second distance is 0.3 microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the first voltage to be about 8.5 volts and the second voltage to be about 4.5 volts and the first distance of the source region is 0.1 microns and the second distance is 0.3 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (1980).

### ***Response to Arguments***

Applicant's arguments filed 26 April 2004 have been fully considered but they are not persuasive. The applicant's argument referring to the prior art not disclosing the programming operation, that is erroneous since the Stewart reference discloses the claimed invention and shows that the source has one voltage, the gate has another and the drain is grounded. In regards to the Stewart reference not being compatible with the Hsu and Gill reference, the Hsu and Gill reference are nonvolatile memory devices and the Stewart reference is a nonvolatile memory device with a control and floating gate

Art Unit: 2822

with a source and drain region. Therefore they are in the same field of endeavor and can be combined together. In regards to the Stewart reference having a Pw transistor, this transistor is just a normal nonvolatile memory device transistor and the Hsu and Gill reference do disclose this transistor in addition the Stewart is biased as claimed to program the device and that is what the claimed invention is doing also. Therefore the rejection stands.

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



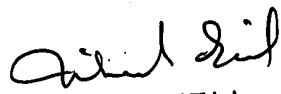
Michael Trinh  
Primary Examiner  
Act SPE

Application/Control Number: 09/777,007

Art Unit: 2822

Page 6

  
KLR

  
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